

## VERIFICATION OF THE TRANSLATION

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Signed by   
Kyung-Duk NAM

Dated this 1st day of June, 2006

[ABSTRACT OF THE DISCLOSURE]

[ABSTRACT]

The present invention relates to an integrated circuit chip in which chip pads are formed in a cell region of a semiconductor substrate and a method for manufacturing the same. The integrated circuit chip comprises a semiconductor substrate having a cell region with integrated circuits and a peripheral circuit region adjacent to each other. A metal layer is formed on the semiconductor substrate and connected to the integrated circuit. A first protection layer is formed over the semiconductor substrate including the metal layer. The first protection layer has a first opening exposing a portion of the metal layer. A redistribution layer is formed over the first protection layer and connected to the metal layer through the first opening. A second protection layer is formed over the redistribution layer and the first protection layer. The second protection layer has a second opening exposing a portion of the redistribution layer. The method for manufacturing an integrated circuit chip comprises forming a metal layer on a cell region of a semiconductor substrate to be electrically connected to integrated circuits, forming a first protection layer on the metal layer leaving a portion of the metal layer exposed, forming a redistribution layer on the first protection layer and connected to the metal layer, and forming a second protection layer on the first protection layer and the redistribution layer leaving a portion of the redistribution layer exposed to define chip pads.

[FIGURE TO BE PUBLISHED]

FIG. 8

[INDEX]

Integrated circuit chip, redistribution layer, rerouting, chip pad, bonding pad

[SPECIFICATION]

[TITLE OF THE INVENTION]

INTEGRATED CIRCUIT CHIP HAVING CHIP PADS FORMING IN A CELL  
5 REGION AND METHOD FOR MANUFACTURING THE SAME

[BRIEF DESCRIPTION OF THE DRAWINGS]

FIG. 1 is a plan view of a conventional center pad type integrated circuit chip;

10 FIG. 2 is a cross-sectional view of the conventional center pad type taken along the line 2-2 of FIG. 1;

FIG. 3 is a plan view of a conventional edge pad type integrated circuit chip;

15 FIG. 4 is a cross-sectional view of the edge pad type chip taken along the line 4-4 of FIG. 3;

FIGS. 5 to 8 are cross-sectional views of an integrated circuit chip illustrating a process of manufacturing an integrated circuit chip according to an embodiment of the present invention;

FIG. 9 is a plan view of the integrated circuit chip shown in FIG. 8;

20 FIG. 10 is an enlarged cross-sectional view of an integrated circuit chip illustrating an alternative configuration of portion A of FIG. 8;

FIG. 11 is a cross-sectional view of the integrated circuit chip of FIG. 9, following wire bonding;

25 FIGS. 12 to 14 are cross-sectional views of an integrated circuit chip illustrating a process of manufacturing an integrated circuit chip according to another embodiment of the present invention;

FIGS. 15 to 17 are cross-sectional views of an integrated circuit chip illustrating a process of manufacturing an integrated circuit chip according to another embodiment of the present invention; and

30 FIG. 18 is a cross-sectional view of an integrated circuit chip according to another embodiment of the present invention.

\* REFERENCE NUMERALS \*

10,30,50; an integrated circuit chip 11,51; a semiconductor substrate

12,52; a metal layer 13,53; a first protection layer

14; an opening 15,55; a redistribution layer

17, 57; a chip pad 18,58; a second protection layer

20a,20b; an interlayer dielectric layer

[DETAILED DESCRIPTION OF THE INVENTION]

[OBJECT OF THE INVENTION]

[FIELD OF THE INVENTION AND RELATED ART]

5 The present invention relates generally to semiconductor devices and method for manufacturing the same and, more particularly, to an integrated circuit chip having chip pads formed on a cell region and to a method for manufacturing the same.

10 The industry is expending significant effort toward forming smaller and thinner chips to meet the demand for high packing density in high-speed, multi-functional semiconductor devices. To reduce chip size, the size of chip pads as well as the pitch between chip pads should be reduced.

15 Typically, an integrated circuit chip having completed a wafer fabrication process has a semiconductor substrate and chip pads formed on the semiconductor substrate. The chip pads serve as input and output terminals of electrical signals. A protection layer formed of nitride is provided on the integrated circuit chip, except for the chip pads. Conventional integrated circuit chips have either a center pad type or an edge pad type structure.

20 FIG. 1 is a plan view of a conventional center pad type integrated circuit chip. FIG. 2 is a cross-sectional view of the conventional center pad type chip taken along line 2-2 of FIG. 1. FIG. 3 is a plan view of a conventional edge pad type integrated circuit chip. FIG. 4 is a cross-sectional view of the conventional edge pad type chip taken along the line 4-4 of FIG. 3.

25 Referring to FIGS. 1 and 2, a center pad type integrated circuit chip 110 comprises a peripheral circuit region  $A_{peri}$  for forming chip pads 112 and cell regions  $A_{cell1}$  and  $A_{cell2}$ . The peripheral circuit region  $A_{peri}$  is formed in the center region of a semiconductor substrate 111. The cell regions  $A_{cell1}$  and  $A_{cell2}$  are formed on the sides of the peripheral circuit region  $A_{peri}$ . Referring to FIGS. 3 and 4, an edge pad type integrated circuit chip 120 comprises peripheral circuit regions  $A_{peri1}$  and  $A_{peri2}$  for forming chip pads 112, and a cell region  $A_{cell}$ . The cell region  $A_{cell}$  is formed in the center region of the semiconductor substrate 121. The peripheral circuit regions  $A_{peri1}$  and  $A_{peri2}$  are formed on the sides of the cell region  $A_{cell}$ . A protection layer 113, 123 is formed over the cell regions and the peripheral circuit regions in both the center and edge pad type chips.

30 In the conventional integrated circuit chips, an additional chip area is needed in peripheral circuit regions for forming chip pads. As a result, the ability to reduce the size of the conventional integrated circuit chips is limited in both chip pad types.

Furthermore, it has been difficult to reduce the bond pad size and the pitch between the chip pads in the conventional semiconductor chips. This is because the chip pads must have a designed minimum size and pitch for electric die sorting (EDS) and to form electrical interconnections.

5 [TECHNICAL SUBJECT TO BE SOLVED]

Accordingly, the present invention is directed to provide an integrated circuit chip in which can overcome the limitation in reducing chip size and a method for manufacturing the same.

The present invention is also directed to provide an integrated circuit chip in which  
10 can overcome the limitation in reducing the size and pitch of chip pads and a method for manufacturing the same.

[CONSTITUTION OF THE INVENTION]

In order to solve the problems, the present invention provide an integrated circuit chip in which chip pads are formed on a cell region of a semiconductor substrate, thereby  
15 incorporating a semiconductor device with a reduced size and an improved reliability, and a method for manufacturing the integrated circuit chip.

The integrated circuit chip comprises a semiconductor substrate having a cell region with integrated circuits and a peripheral circuit region adjacent to each other. A metal layer is formed on the semiconductor substrate and connected to the integrated circuit. A first  
20 protection layer is formed over the semiconductor substrate including the metal layer. The first protection layer has a first opening exposing a portion of the metal layer. A redistribution layer is formed over the first protection layer and connected to the metal layer through the first opening. A second protection layer is formed over the redistribution layer and the first protection layer. The second protection layer has a second opening exposing a portion of the  
25 redistribution layer.

The integrated circuit further comprises an interlayer dielectric layer interposed between the first protection layer and the second protection layer. The interlayer dielectric layer is formed over the first protection layer or on a portion of the first protection layer to be connected to the chip pad of the redistribution layer.

30 The first protection layer is fabricated from a high-density plasma silicon oxidized layer and the second protection layer is fabricated from at least one selected from a group consisting of a high-density plasma silicon oxidized layer and a polyimide layer.

The method for manufacturing an integrated circuit chip comprises (a) forming a metal layer on a cell region of a semiconductor substrate to be electrically connected to

integrated circuits, (b) forming a first protection layer over the metal layer leaving a portion of the metal layer exposed, (c) forming a redistribution layer over the first protection layer to be connected to the metal layer, and (d) forming a second protection layer over the first protection layer and the redistribution layer leaving a portion of the redistribution layer exposed.

The method further comprises forming an interlayer dielectric layer over the first protection layer and forming a redistribution layer on the interlayer dielectric layer, after forming the first protection layer. Thereby the interlayer dielectric layer is interposed between the first protection layer and the second protection layer. The interlayer dielectric layer is formed over the first protection layer or on a portion of the first protection layer to be connected to the chip pad of the redistribution layer.

The method comprises forming a high-density plasma silicon oxidized layer for forming the first protection layer, and forming at least one selected from a group consisting of forming a high-density plasma silicon oxidized layer and forming a polyimide layer for forming the second protection layer.

The example embodiments of the present invention will be readily understood with reference to the following detailed description thereof in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements.

## 20 FIRST EMBODIMENT

FIGS. 5 to 8 are cross-sectional views of an integrated circuit chip illustrating a process of manufacturing an integrated circuit chip according to a first embodiment of the present invention. FIG. 9 is a plan view of the integrated circuit chip shown in FIG. 8. FIG. 10 is an enlarged cross-sectional view of an integrated circuit chip illustrating an alternative configuration of portion A of FIG. 8. FIG. 11 is a cross-sectional view of the integrated circuit chip of FIG. 9, following wire bonding.

Referring to FIGS. 8 and 9, an integrated circuit chip 10 comprises a semiconductor substrate 11 having integrated circuits formed thereon. In particular, the semiconductor substrate 11 includes a peripheral circuit region  $A_{peri}$  formed in the center region thereof and cell regions  $A_{cell1}$  and  $A_{cell2}$  arranged on the sides of the peripheral circuit region  $A_{peri}$ . A metal layer 12 is formed in a predetermined area of the substrate 11 and connected to the integrated circuits. The metal layer 12 is preferably formed in a center region of the semiconductor substrate 11. One end of the metal layer 12 is preferably formed on the portion of the peripheral circuit region  $A_{peri}$ . In the conventional integrated circuit chip, an

additional chip area is needed in peripheral circuit regions for forming chip pads having a minimum size and pitch designed for electric die sorting (EDS) and making electrical interconnections. According to the forgoing embodiment of the present invention, however, no larger additional area for forming chip pads is required, rather only the small portion of the metal layer 12 needs to be formed on the peripheral circuit region  $A_{peri}$ . The remaining portion of the metal layer 12 extends across a portion of the cell region according to an embodiment of the present invention. The width of the semiconductor substrate 11 can therefore be reduced by approximately the width of the chip pad area of the conventional integrated circuit chip. According to another aspect of the present invention, the metal layer 12 can alternatively be formed entirely within the peripheral circuit region. Also, the metal layer 12 can be formed entirely within the cell region (although not shown). The metal layer 12 can be made of a metal having excellent electrical conductivity, such as aluminum (Al).

A first protection layer 13 is then formed on the metal layer 12 to expose predetermined portions of the metal layer 12. The first protection layer 13 is made of a material having good insulation and integration properties to protect chip pads 17 from mechanical stress due to subsequent wire bonding, beam lead bonding, or ball bonding. For example, a high-density plasma (HDP) oxidized layer may be used as the first protection layer 13. An HDP oxide layer using silan, oxygen and argon gases, for example, an HDP-SiO<sub>2</sub> layer is preferably used.

A redistribution layer 15, having a predetermined layout, is formed on the first protection layer 13. One end of the redistribution layer 15 is electrically connected to the exposed portion of the metal layer 12 and the other end of the redistribution layer 15 is formed having a predetermined size on the cell region. As shown in portion "A" of FIG. 8, the first protection has openings which are filled with the redistribution layer 15. An alternative configuration of portion A of FIG. 8 is illustrated in FIG. 10. The redistribution layer 15 preferably comprises three layers. These three layers can, for example, include a titanium (Ti) layer having a thickness of about 300 to 500Å, an aluminum (Al) layer having a thickness of about 15,000Å, and a titanium nitride (TiN) layer having a thickness of about 300 to 500Å. The redistribution layer 15 may be formed of copper (Cu), aluminum (Al), zinc (Zn), iron (Fe), platinum (Pt), cobalt (Co), lead (Pb), nickel (Ni), or an alloy of these elements.

A second protection layer 18 is formed on the redistribution layer 15. A predetermined portion of the redistribution layer 15 is exposed through the second protection layer 18 to define the chip pads 17. The chip pads 17 are preferably flush with the

- redistribution layer 15. The chip pads 17 are disposed above at least part of the cell regions  $A_{cell1}$ ,  $A_{cell2}$  of the substrate 11. As shown in FIG. 11, electrical connection means such as bonding wires 99 are coupled to the chip pads 17. If necessary, the positions of chip pads 17 can be adjusted depending on the design and structure of the electrical interconnections.
- 5 Although the chip pads 17 shown in FIG. 9 are disposed in a single row along opposing edges of the substrate 11, the pads 17 may be disposed along all four edges or in a zigzag shape. The second protection layer 18 may be an HDP oxide layer such as an HDP-SiO<sub>2</sub> layer. The second protection layer 18 may further comprise a polyimide layer on the HDP-SiO<sub>2</sub> layer so as to protect integrated circuits from alpha particles.
- 10 According to one embodiment, the redistribution layer 15 reroutes the chip pads 17 from the metal layer 12 in the peripheral circuit region  $A_{peri}$  to above the cell regions  $A_{cell1}$  and  $A_{cell2}$ . As shown above, one end of the redistribution layer 15 is electrically connected to the exposed metal layer 12 via openings. The other end extends toward the edge of the substrate 11. In other words, according to one aspect of the present invention, the portion of the metal layer 12 extends substantially from the center region of the semiconductor substrate 11 toward an edge of the semiconductor substrate 11. The chip pads 17 can therefore be formed along sides of the semiconductor substrate 11.
- 15 Thus, according to various embodiments of the present invention, edge pad type semiconductor chips can be fabricated using center pad type semiconductor chips, which are known to have improved electrical performance characteristics over the peripheral pad type chips. The pitch between the bond pads can increase. During the EDS test, a probe can easily contact the bond pads. These modified peripheral pad chips thus need not be packaged in a lead-on-chip (LOC) type package, but may be implemented in a conventional package.
- 20 As described above, the chip pads 17 of this embodiment are preferably formed over at least a part of the cell regions of the substrate 11. Therefore, the peripheral circuit region  $A_{peri}$  has a much smaller width than that of the conventional peripheral circuit region. Thus, the total width of the integrated circuit chip 10 can be reduced. The widths of the cell regions  $A_{cell1}$ <sup>1</sup> and  $A_{cell2}$  may be the same as that of the conventional cell region. Of course, the total thickness of the semiconductor chip 10 increases due to the formation of the redistribution
- 25 layer 15 and the insulating layer 18 above the cell regions  $A_{cell1}$  or  $A_{cell2}$ . The increased percentage in total thickness of the chip 10 is no more than the reduced percentage of the total width of the chip 10. The total size of the chip 10 can be therefore reduced.

30 A method of manufacturing the above-described semiconductor chip 10 will now be described.

Referring to FIG. 5, a semiconductor substrate 11 includes on-chip circuits formed on the cell regions  $A_{cell1}$ ,  $A_{cell2}$  and the peripheral circuit region  $A_{peri}$ . The metal layer 12 is formed on the substrate 11 to be selectively connected to the integrated circuits. The metal layer 12 is formed in a predetermined layout using conventional techniques such as a plating method or a deposition method including sputtering. As described above, although the metal layer 12 can be formed on both the cell regions  $A_{cell1}$ ,  $A_{cell2}$  and the peripheral circuit region  $A_{peri}$ , the metal layer may be formed just the cell regions  $A_{cell1}$ ,  $A_{cell2}$  (not shown).

Next, as shown in FIG. 6, a first protection layer 13 is formed on the metal layer 12. Openings 14 are formed to expose predetermined portions of the metal layer 12. The protection layer 13 is made of a material such as HDP-SiO<sub>2</sub> having good integration and insulating qualities. Although the forgoing embodiment comprises a single protection layer, the present invention may comprise two or more protection layers. In this case, the planarization process is preferably performed on the protection layer to improve the planarity of the protection layer 13. Accordingly, the planarity of the redistribution layer 15 thereon can be in turn improved. The planarization process is performed using chemical mechanical polishing. The integrated circuits under the protection layer 13 can therefore be protected from physical stresses during the formation of electrical interconnections. The protection layer 13 also helps planarize the underlying structure. The openings 14 can be formed above either the cell regions  $A_{cell1}$ ,  $A_{cell2}$  or the peripheral circuit region  $A_{peri}$ .

Referring to FIG. 7, the redistribution layer 15 is formed on the first protection layer 13 and the protection layer 13. The redistribution layer 15 fills the openings 14 and is electrically connected to the metal layer 12. The redistribution layer 15 is obtained in a desired layout using a plating method or a deposition method including sputtering, for example.

Referring to FIG. 8, a second protection layer 18 is formed on the redistribution layer 15, exposing predetermined portions of the redistribution layer 15. The exposed portions of the redistribution layer 15 are defined as the chip pads 17. The second protection layer 18 is preferably made of HDP-SiO<sub>2</sub> to protect the integrated circuits from mechanical stresses. The second protection layer 18 may further comprise a polyimide layer on the HDP-SiO<sub>2</sub> layer to protect the integrated circuits from alpha particles.

## SECOND EMBODIMENT

FIGS. 12 to 14 are cross-sectional views of an integrated circuit chip illustrating a process of manufacturing an integrated circuit chip according to a second embodiment of the

present invention. In this embodiment, as shown in FIG. 14, an integrated circuit chip 30 further comprises an interlayer dielectric (ILD) 20a on a first protection layer 13. A redistribution layer 15 is formed on the ILD 20a. The ILD 20a can be interposed between the protection layer 13 and the redistribution layer 15, and the electrical properties of the 5 semiconductor chips 30 are improved. The capacitance, for example, can be lowered. The thickness of the ILD 20a is between 2 to 50  $\mu\text{m}$ , for example determined base on the capacitance and the intensity supplement. The ILD 20a may be made of polyimide, polybenzoxazole (PBO), benzocyclobutene (BCB), epoxy, and so on.

As shown in FIG. 12, a semiconductor substrate 11 includes a metal layer 12 10 preferably formed on at least a portion of the peripheral circuit region  $A_{\text{peri}}$  and electrically connected thereto. A first protection layer 13 is formed over the semiconductor substrate 11 including the metal layer 12. An ILD 20a is then formed over the first protection layer 13 using conventional techniques, for example a spin coating method and a photo process. Openings are formed through the first protection layer 13 and the ILD 20a to expose portions 15 of the metal layer 12. As shown in FIG. 13, a redistribution layer 15 is formed on the ILD 20a and within the opening and is electrically connected to the metal layer 12. As shown in FIG. 14, a second protection layer 18 is formed over the redistribution layer 15. The ILD 20a and the second protection layer 18 are fabricated from polyimide.

20 THIRD EMBODIMENT

FIGS. 15 to 17 are cross-sectional views of an integrated circuit chip illustrating a process of manufacturing an integrated circuit chip according to a third embodiment of the present invention.

Referring to FIG. 17, an integrated circuit chip 50 is similar to the integrated circuit 25 chip 30 of the second embodiment, except for having chip pads 17 formed on a first protection layer 13. Thereby the integrated circuit chip 50 may reduce a cushion phenomenon may be caused by physical stresses during formation of electrical interconnections.

As shown in FIG. 15, an ILD 20b is formed over the first protection layer 13 exposing predetermined portions of the first protection layer 13 corresponding to the chip pads 17. As 30 shown in FIG. 16, a redistribution layer 15 is formed on the ILD 20b and within openings. As shown in FIG. 17, predetermined portions of the redistribution layer 15 is exposed through a second protection layer 18 to define the chip pads 17.

#### FOURTH EMBODIMENT

FIG. 18 is a cross-sectional view of an integrated circuit chip according to a fourth embodiment of the present invention.

Referring to FIG. 18, an integrated circuit chip 70 comprises a semiconductor substrate 51 having integrated circuits formed thereon. In particular, the semiconductor substrate 51 includes a cell region  $A_{cell}$  formed in the center region thereof and peripheral circuit regions  $A_{peri1}$  and  $A_{peri2}$  arranged on the sides of the cell region  $A_{cell}$ . A metal layer 52 is formed on the semiconductor substrate 11 to be connected to integrated circuits. A first protection layer 53 is formed over the metal layer 52. A redistribution layer 55 is formed on the first protection layer to be connected to the metal layer 52. A second protection layer 58 is formed over the redistribution layer 55. Predetermined portions of the redistribution layer 55 are exposed through the second protection layer 58 to define chip pads 57. The chip pads 57 are disposed above the cell region  $A_{cell}$  of the substrate 51.

According to the forgoing embodiment of the present invention, however, no larger additional area for forming chip pads is required, rather only the small portion of the metal layer 12 needs to be formed on the peripheral circuit region  $A_{peri}$ . The width of the semiconductor substrate 11 can therefore be reduced by approximately the width of the chip pad area of the conventional integrated circuit chip. The metal layer 52 can alternatively be formed entirely within the cell region  $A_{cell}$ .

Thus, according to various embodiments of the present invention, edge pad type semiconductor chips can be fabricated using center pad type semiconductor chips, which are known to have improved electrical performance characteristics over the peripheral pad type chips.

Although various preferred embodiments of the present invention have been disclosed herein for illustrative purposes, those skilled in the art will appreciate that various modifications, additions, and substitutions are possible without departing from the scope and spirit of the invention as provided in the accompanying claims. For example, a semiconductor device may comprise a semiconductor substrate having a cell region and peripheral circuit regions with chip pads. Connectors may connect the chip pads to integrated circuits. A redistribution layer may be formed to be connected to the connectors and be configured to reroute the chip pads to above the cell region. The chip pads on the peripheral circuit regions may be separated from the semiconductor substrate.

#### [EFFECT OF THE INVENTION]

In accordance with the embodiments of the present invention, a redistribution layer may reroute chip pads from a metal layer in a peripheral circuit region to above a cell region. Therefore, the peripheral circuit region has a much smaller width than that of the conventional peripheral circuit region. Thus, the total width of the integrated circuit chip can  
5 be reduced. Thereby a larger number of integrated circuit chips can be obtained from a conventional wafer.

According to various embodiments of the present invention, edge pad type integrated circuit chips can be fabricated using center pad type integrated circuit chips, which are known to have improved electrical performance characteristics over the edge pad type chips. These  
10 modified edge pad chips thus need not be packaged in a lead-on-chip (LOC) type package, but may be implemented in a conventional package.

Further, the pitch between chip pads can increase. During the EDS test, a probe can easily contact the chip pads.

A first protection layer is made of a material having good insulation, for example,  
15 HDP-SiO<sub>2</sub> and integration properties to protect chip pads from mechanical stress due to subsequent wire bonding, beam lead bonding, or ball bonding. may be used as the first protection layer.

WHAT IS CLAIMED IS:

1. An integrated circuit chip having chip pads, the integrated circuit chip comprising:
  - a semiconductor substrate having a cell region with integrated circuits and a peripheral circuit region adjacent to each other;
  - a metal layer formed on the semiconductor substrate and connected to the integrated circuit;
  - a first protection layer formed on the semiconductor substrate including the metal layer, the first protection layer having a first opening exposing a portion of the metal layer;
  - 10 a redistribution layer formed on the first protection layer and connected to the metal layer through the first opening; and
  - a second protection layer formed on the redistribution layer and the first protection layer, the second protection layer having a second opening exposing a portion of the redistribution layer to define the chip pads.
- 15 2. The integrated circuit chip of claim 1, wherein the semiconductor substrate is formed of a center pad type integrated circuit design and the chip pads are formed along the periphery of the cell region of the semiconductor substrate.
- 20 3. The integrated circuit chip of claim 1, wherein the semiconductor substrate is formed of an edge pad type integrated circuit design and the chip pads are formed on the cell region in the center of the semiconductor substrate.
- 25 4. The integrated circuit chip of claim 1, wherein the first protection layer is fabricated from a high-density plasma oxidized layer.
5. The integrated circuit chip of claim 4, wherein the first protection layer is fabricated from a high-density plasma silicon oxidized layer.
- 30 6. The integrated circuit chip of claim 1, wherein the second protection layer is fabricated from at least one selected from a group consisting of a high-density plasma silicon oxidized layer and a polyimide layer.

7. The integrated circuit chip of claim 1, further comprising an interlayer dielectric interposed between the first protection layer and the second protection layer.

8. The integrated circuit chip of claims 1 or 7, wherein the chip pad contacts the first  
5 protection layer through the interlayer dielectric.

9. The integrated circuit chip of claim 1, wherein the second protection layer is fabricated from polyimide.

10 10. The integrated circuit chip of claim 1, wherein the metal layer is formed entirely within the cell region of the semiconductor substrate.

11. The integrated circuit chip of claim 1, wherein the metal layer extends from the cell region to the peripheral circuit region.

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12. An integrated circuit chip comprising:

a semiconductor substrate formed of a center pad type integrated circuit design, the semiconductor substrate having a cell region with integrated circuits and peripheral circuit regions adjacent to each other;

20 a metal layer formed on the semiconductor substrate and connected to the integrated circuit;

a first protection layer formed on the semiconductor substrate including the metal layer, the first protection layer having a first opening exposing a portion of the metal layer;

25 a redistribution layer formed on the first protection layer and connected to the metal layer through the first opening; and

a second protection layer formed on the redistribution layer and the first protection layer, the second protection layer having a second opening exposing a portion of the redistribution layer located along the periphery of the cell region of the semiconductor substrate to define chip pads.

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13. A method for manufacturing an integrated circuit chip, the method comprising:

forming a metal layer on a cell region of a semiconductor substrate to be electrically connected to integrated circuits;

forming a first protection layer over the metal layer leaving a portion of the metal layer exposed;

forming a redistribution layer over the first protection layer to be connected to the metal layer; and

5 forming a second protection layer over the first protection layer and the redistribution layer leaving a portion of the redistribution layer exposed to define the chip pads.

14. The method of claim 13, wherein forming the first protection layer includes forming an interlayer dielectric over the first protection layer, except for the exposed portion of the  
10 metal layer.

15. The method of claims 13 or 14, wherein forming the interlayer dielectric layer includes removing portions of the interlayer dielectric corresponding to the chip pads of the redistribution layer.

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16. The method of claim 13, wherein forming the second protection layer includes at least one selected from a group consisting of forming a high-density silicon oxidized layer and forming a polyimide layer.